Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An asynchronous transfer mode (ATM) cell switching method, comprising:

a) dividing an input ATM adaptation layer 2 (AAL2) cell into AAL2 type common part sublayer (CPS) packets;

b) sequentially storing the divided CPS packets into first storage areas and sequentially storing first identifiers of the first storage areas;

c) reading the stored CPS packets in the order of the stored first identifiers, sequentially storing the read CPS packets in second storage areas used to route the CPS packets to each destination, and sequentially storing second identifiers of the second storage areas; and

d) reading the CPS packets, in the order of the second identifiers, from the second storage areas and multiplexing the read CPS packets to generate a reconstructed AAL2 cell.

2. (Currently amended) The ATM cell switching method of claim 1, wherein ~~step c~~) further comprises:

changing origination channel identifiers (CIDs) of the read CPS packets to

corresponding destination CIDs; and

sequentially storing the read CPS packets in the second storage areas corresponding to the destination CIDs.

3. (Original) The ATM cell switching method of claim 1, wherein the CPS packets are stored in the first and second storage areas according to their respective order of arrival.

4. (Original) The ATM cell switching method of claim 1, wherein the CPS packets are read from the first and second storage areas according to their respective order of storage.

5. (Currently amended) The ATM cell switching method of claim 1, wherein

the divided CPS packets are stored in the first storage areas, in accordance with corresponding virtual paths/virtual channels (VPs/VCs) of the respective CPS packets; and

the CPS packets read in ~~step c~~) are stored in the second storage areas, in accordance with respective channel identifiers (CIDs).

6. (Original) The ATM cell switching method of claim 5, further comprising: generating a first reference table that maps each of the first identifiers with the corresponding virtual path/virtual channel (VP/VC); and

generating a second reference table that maps each of the second identifiers with the corresponding channel identifier (CID).

7. (Original) The ATM cell switching method of claim 5, wherein the first and second identifiers are stored in the order that the CPS packets are stored to the corresponding first and second storage areas, respectively.

8. (Original) The ATM cell switching method of claim 5, wherein the CPS packets are read from the first and second storage areas according to their respective order of storage.

9. (Original) The ATM cell switching method of claim 5, further comprising implementing a switching test by reading the CPS packets from the second storage areas in the order of the second identifiers and comparing the read CPS packets to a standard.

10. (Original) The ATM cell switching method of claim 5, further comprising implementing a switch signaling by reading the CPS packets from the second storage areas in the order of the second identifiers and outputting the read CPS packets to a processor.

11. (Original) The ATM cell switching method of claim 5, further comprising routing

the CPS packets stored in the first storage areas to another switch in the order of the first identifiers.

12. (Original) The ATM cell switching method of claim 5, wherein the first and second storage areas have a queue type structure.

13. (Currently amended) The ATM cell switching method of claim 5, wherein ~~step c~~) further comprises:

changing origination CIDs of the read CPS packets to corresponding destination CIDs; and

sequentially storing the read CPS packets in the second storage areas corresponding to the destination CIDs.

14. (Currently amended) An asynchronous transfer mode (ATM) cell switching system, comprising:

a reassembly processing unit that divides an input ATM adaptation layer 2 (AAL2) cell into AAL2-type common part sublayer (CPS) packets;

a first memory that sequentially stores the divided CPS packets into first storage areas and sequentially stores first identifiers of the first storage areas;

a CPS packet switching unit that reads the stored CPS packets from the first storage areas in the order of the stored first identifiers and routes the read CPS packets to each destination;

a second memory that sequentially stores the routed CPS packets into second storage areas and sequentially stores second identifiers of the second storage areas; and

an assembly processing unit that reads the CPS packets from the second storage areas in the order of the second identifiers and multiplexes the CPS packets read from the second storage areas to generate a reconstructed AAL2 ~~cell~~cell,

wherein the CPS packet switching unit changes origination channel identifiers (CIDs) of the CPS packets read from the first storage areas to corresponding destination CIDs and sequentially stores the read CPS packets in the second storage areas corresponding to the destination CIDs.

15. (Canceled)

16. (Original) An asynchronous transfer mode (ATM) cell switching system, comprising:

first, second, third, and fourth memories that sequentially store ATM adaptation layer 2 (AAL2) type common part sublayer (CPS) packets and output the CPS packets in the

order of their respective storage, wherein each memory has storage areas;

a reassembly processing unit that divides an input AAL2 cell into the AAL2 type CPS packets, stores the divided CPS packets in different first storage areas of the first memory in accordance with corresponding virtual paths/virtual channels (VPs/VCs), and stores first identifiers of the different first storage areas in the second memory;

a CPS packet switching unit that reads the CPS packets stored in the first memory in the order of the first identifiers stored in the second memory, stores the read CPS packets in different second storage areas of the third memory in accordance with corresponding destination channel identifiers (CIDs), and stores second identifiers of the second storage areas in the fourth memory; and

an assembly processing unit that reads the CPS packets stored in the third memory in the order of the second identifiers stored in the fourth memory and multiplexes the read CPS packets to generate a reconstructed AAL2 cell.

17. (Original) The ATM cell switching system of claim 16, further comprising:

a first reference table that maps the first identifiers with the corresponding VPs/VCs; and

a second reference table that maps the second identifiers with the corresponding destination CIDs.

18. (Original) The ATM cell switching system of claim 17, wherein the reassembly processing unit refers to the first reference table to determine the first storage areas corresponding to the VPs/VCs of the CPS packets.

19. (Original) The ATM cell switching system of claim 17, wherein the CPS packet switching unit refers to the second reference table to determine the respective destination CIDs corresponding to the CPS packets.

20. (Original) The ATM cell switching system of claim 19, wherein the CPS packet switching unit changes origination CIDs of the CPS packets read from the first memory to the corresponding destination CIDs, with reference to the second reference table.

21. (Original) The ATM cell switching system of claim 16, wherein the first and second identifiers are stored in the order that the CPS packets are stored to the corresponding first and second storage areas, respectively.

22. (Original) The ATM cell switching system of claim 16, wherein the first, second, third, and fourth memories have a queue type structure.

23. (Original) The ATM cell switching system of claim 16, further comprising:

a central processing unit that reads the CPS packets from the first memory in the order of the stored first identifiers and implements testing and signaling for switching.

24. (Original) The cell switching system of claim 23, wherein the first, second, third, and fourth memories have a queue type structure.

25. (Currently amended) The ATM cell switching system of claim 16, further comprising:

a plurality of cell switches that ~~each have~~each has first, second, third, and fourth memories, a reassembly processing unit, a CPS packet switching unit, and an assembly processing unit; and

a router that routes the CPS packets output from one of the plurality of cell switches to another cell switch.

26. (Original) The cell switching system of claim 25, wherein the first, second, third, and fourth memories have a queue type structure.

27. - 28. (Canceled)